THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte KIYOHIRO FURUTANI and HIDEYUKI OZAKI

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Appeal No. 96-2950[1]
Application 08/145,710

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ON BRIEF

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Before HAIRSTON, FLEMING and CARMICHAEL, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of

[1]Application for patent filed November 4, 1993.

claims 1 through 4 and 8 through 11. Claims 6, 7 and 12 through 15 have been canceled. Claim 5 has been objected to for being dependent upon a rejected claim. Claims 16 and 17 have been allowed.

The invention relates to output driver circuits that suppress noise generation for semiconductor integrated circuit devices.

Independent claim 1 is reproduced as follows:

1. An output driver circuit including a data output terminal and for providing an output data via said data output terminal, comprising:

a semiconductor substrate,

a predetermined node formed in said substrate,

current providing means formed in said substrate and responsive to an applied data signal defining said output data for providing an output current via said data output terminal, and

current increasing rate control means formed in said substrate and responsive to a potential at said predetermined node for controlling an increasing rate of the output current by said current providing means,

wherein said current providing means comprises a first field effect transistor connected between a first power supply potential and said data output terminal, and said current increasing rate control means comprises conductance increasing

timing control means responsive to the potential at said predetermined node for controlling an increasing rate of a conductance of said first field effect transistor, and

said current increasing rate control means controlling the output driver circuit to operate in at least a first state and a second state, said current providing means provides a first current increasing rate in the first state and said current providing means provides a second current increasing rate in the second state, said second current increasing rate being slower than said first current increasing rate.

The references relied on by the Examiner are as follows:

Davis	4,961,010	Oct. 2, 1990
Kohda	5,003,205	Mar. 26, 1991

Claims 1 through 4 and 9 through 11 stand rejected under 35 U.S.C. § 102 as being anticipated by Davis. Claims 1, 2 and 8 stand rejected under 35 U.S.C. § 102 as being anticipated by Kohda. In the Examiner's answer, the Examiner sets forth a new ground of rejection that claims 2, 3, 8 and 11 are indefinite under 35 U.S.C. § 112, second paragraph. The Appellants respond to the new ground of rejection by filing on February 7, 1996 an amendment which amends claims 2, 3, 8 and 11. In the supplemental Examiner's answer, the Examiner states that the

amendment has been entered and that the rejection under 35 U.S.C. § 112, second paragraph, has been withdrawn. In a later letter, the Examiner states that claims 2, 3, 8 and 11 are rejected under 35 U.S.C. § 112, second paragraph, without any further explanation of the basis. It is unclear whether the Examiner mistakenly made this statement or that the Examiner intended to reinstate the rejection. After reviewing the record, including the Examiner's rejection, Appellants' amendment to the claims, as well as Appellants' arguments, we find that the Examiner mistakenly repeated this withdrawn rejection in the later letter.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the briefs[2] and the answers[3] for

[2]Appellants filed an appeal brief on November 9, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on February 7, 1996. We will refer to this reply appeal brief as the reply brief. The Examiner responded to the reply brief in a supplemental Examiner's answer dated February 23, 1996. We note that the reply brief has been entered into the record.

[3]The Examiner responded to the brief with an Examiner's answer dated December 13, 1995. We will refer to the Examiner's answer as simply the answer. The Examiner responded to the reply

the details thereof.

OPINION

After a careful review of the evidence before us, we do not agree with the Examiner that claims 1 through 4 and 8 through 11 are anticipated by the applied references.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co***., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

Appellants' claim 1 recites

> current increasing rate control means formed in said substrate and responsive to a potential at said predetermined node for controlling an increasing rate of the output current by said current providing means, wherein . . . said current increasing rate control means comprises conductance increasing timing control means responsive to the potential at said predetermined node for controlling an increasing rate of a conductance of said first field effect transistor, and said current increasing rate control means controlling the output driver circuit to operate in at least a first state and a second state, said current providing

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brief with a supplemental Examiner's answer dated February 23, 1996. We will refer to the supplemental Examiner's answer as simply the supplemental answer.

> means provides a first current increasing rate in the first state and said current providing means provides a second current increasing rate in the second state, ***said second current increasing rate being slower than said first current increasing rate***. [Emphasis added.]

Appellants argue on pages 7 and 8 of the brief that neither Davis nor Kohda teaches the Appellants' claimed limitations as required under 35 U.S.C. § 102. In particular, Appellants argue that Davis does not disclose two different states as well as provide a second current increasing rate that is slower than the first current increasing rate. Appellants further argue that although Kohda does disclose two different states, Kohda does not disclose a second current increasing rate being slower than the first current increasing rate.

On page 4 of the answer, the Examiner argues that Davis teaches a current increasing rate control means shown as elements R2, 44 and P2 in Figure 1. However, the Examiner does not respond to Appellants' arguments that Davis does not teach two different states or that the current increasing rate control means provides a second current increasing rate that is slower than the first current increasing rate.

Upon a careful review of Davis, we fail to find that Davis teaches

> current increasing rate control means formed in said substrate and responsive to a potential at said predetermined node for controlling an increasing rate of the output current by said current providing means, wherein . . . said current increasing rate control means comprises conductance increasing timing control means responsive to the potential at said predetermined node for controlling an increasing rate of a conductance of said first field effect transistor, and said current increasing rate control means controlling the output driver circuit to operate in at least a first state and a second state, said current providing means provides a first current increasing rate in the first state and said current providing means provides a second current increasing rate in the second state, said second current increasing rate being slower than said first current increasing rate

as recited in Appellants' claim 1. Furthermore, we note that claims 2 through 4 and 9 through 11 are dependent on claim 1 and thereby recite the above limitation. Therefore, we find that Davis fails to teach all of the limitations of claims 1 through 4 and 9 through 11, and thereby the claims are not anticipated by Davis.

On pages 5 and 6 of the answer, the Examiner argues that Kohda teaches a current increasing rate control means shown as element 6 in Figure 1. On page 8 of the answer, the Examiner responds to the Appellants' argument by stating that the limitation of having different current increasing rates is interpreted broadly to mean that the circuit has different current flows.

Appellants respond on page 3 of the reply brief that Appellants' claim 1 recites "second current increasing rate being slower than the first current increasing rate." Appellants argue that Appellants' independent claim 1 recites that the current increasing rate refers to the speed or rate of change of the current and not the quantity of the current. We agree and find that Appellants' claim 1 requires that the rate of increasing change of the second current is slower than the rate of increasing change of the first current.

In the supplemental answer, the Examiner argues that Kohda in lines 4-9 of column 8 suggests that current increasing rate can be varied wherein one is slower than another one. Even if this is true, the Examiner has made an anticipation rejection which requires a showing of a teaching of the Appellants' limitation. The question of whether one of ordinary skill in the art would have reason to modify Kohda's teaching is not a question before us for our consideration.

Upon a careful review of Kohda, we fail to find that Kohda teaches

> current increasing rate control means formed in said substrate and responsive to a potential at said predetermined node for controlling an increasing rate of the output current by said current providing means, wherein ... said current increasing rate control means comprises conductance increasing timing control means responsive to the potential at said predetermined node for controlling an increasing rate of a conductance of said first field effect transistor, and said current increasing rate control means controlling the output driver circuit to operate in at least a first state and a second state, said current providing means provides a first current increasing rate in the first state and said current providing means provides a second current increasing rate in the second state, said second current increasing rate being slower than said first current increasing rate

as recited in Appellants' claim 1. Furthermore, we note that claims 2 and 8 are dependent on claim 1 and thereby recite the above limitation. Therefore, we find that Kohda fails to teach all of the limitations of claims 1, 2 and 8, and thereby the claims are not anticipated by Kohda.

In view of the foregoing, the decision of the Examiner

rejecting claims 1 through 4 and 8 through 11 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)	

Appeal No. 96-2950
Application 08/145,710

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